ABSTRACT OF THE DISCLOSURE

There is provided a shift register circuit of a wide operation margin capable of reducing a capacitive load of a clock signal line, reducing a load of external circuits and achieving consumption power reduction and cost reduction with a simple construction, and an imaging display device including it. A plurality of serially connected register blocks BLK2 has a D-type flip-flop DFF1 that operates in synchronization with a clock signal, transfer gates TG11 and TG12 for controlling clock signals CK and /CK supplied to the D-type flip-flop DFF1 and an exclusive-OR circuit XOR1 that outputs a control signal to the transfer gates TG11 and TG12 so that the transfer gates are brought into an ON-state only in a specified period during which the output of the D-type flip-flop DFF1 changes i.e. when the input signal level and the output signal level of the D-type flip-flop DFF1 differ from each other.